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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,365	12/01/2003	Mitsuaki Osame	12732-183001 / US6776	8069

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EXAMINER	
NGUYEN, LONG T	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,365	OSAME ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7,8,11,12,43,44,53,54,65,66,68-71,73 and 74* is/are allowed.

6)☒ Claim(s) *1,2,14,15,20,21,24,25,30,31,37,38,47,48,57-64,67,72 and 75-96* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/29/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 1,2,7,8,11,12,14,15,20,21,24,25,30,31,37,38,43,44,53,54 and 57-96.

DETAILED ACTION

Claim Objections

1. Claims 75-96 are objected to because of the following informalities:

Claims 75, 80, 85 and 91, line 2, "a first and a second circuit:" should be changed to --a first circuit and a second circuit,--.

Claims 76-79, 81-84, 86-90 and 92-96 are objected to because they include the informality of claims 75, 80, 85 and 91, respectively.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 14, 15, 20, 21, 24, 25, 30, 31, 58, 62, 67, 72, and 75-96 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 14, the recitation "a first sampling pulse from a first circuit of a preceding stage" on line 2-3 and "a second sampling pulse from a second circuit of a present stage" on line 3-4 cause the claim to be indefinite it is not clear where the first and second circuits come from, and whether the first and second circuits are part of the data latch circuit, and it is also not clear "a preceding stage" and "a present stage" of what.

Claims 15, 20 and 21 are indefinite the similar reasons as discussed in claim 14.

With respect to claim 24, the phrase "the potential difference of a power supply" is indefinite because "the potential difference" lacks antecedent basis, and it is not clear whether

the above phrase means 'a potential of a power supply' since it is not understood how a potential difference can be determined when there is only one power supply (i.e., a power supply voltage recited in the claim). Note that, it is required two power supplies to determined the potential difference. Clarification and/or appropriate correction is required.

Claims 25, 30, 31, 58, 62, 67 and 72 are indefinite the similar reasons as discussed in claim 24.

With respect to claims 75, this claim is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: there is no connection between the shift register and the at least first and second data latch circuits, so it is not clear how they are related to each other.

Claims 76-79 are indefinite because they include the indefiniteness of claim 75.

Also in claim 76, "of a preceding stage" on line 2 and "of a present stage" on line 3-4 cause the claim to be indefinite because it is not clear "a preceding stage" and "a present stage" of what.

Claim 77 is also indefinite for the same reasons as discussed in claim 24.

Claims 80, 85 and 91 are indefinite for the same reason as in claim 75.

Claims 81-84, 86-90 and 92-96 are indefinite because they include the indefiniteness of claims 80, 85 and 91, respectively.

Note that claims 81, 87 and 93 are also indefinite for the same reason as in claim 76.

Note that claims 82, 88 and 94 are also indefinite the same reasons as in claim 24.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 2, 14, 15, 24, 25, 37, 38, 47, 48 and 57-64 are rejected under 35 U.S.C. 102(e) as being anticipated by Tam (USP 6,628,146).

With respect to claims 1, 24, 37, 47, 57-60 Figure 3 of Tam discloses a data latch circuit for sampling a digital signal (Vin2, see Figure 4 in which input waveform is a digital input signal), which includes: a capacitor means (C2) having first and second electrodes (right electrode and left electrode of C2); an inverter (Q1, Q11); a switch (Q6) wherein the switch (Q6) is turned on and a first potential is input to the second electrode of the capacitor means (when Q6 is turned on, so Q8 is also on to connected the second electrode of C2 to ground) during a reset period; and the digital signal (Vin2) is input to the second electrode of the capacitor means (C2) during a sampling period (Q6 is off, and Q10 is ON) after the reset period. Note that the circuit in Figure 3 of Tam uses thin-film transistors and are used in display device (see lines 47 to line 60 of Col. 5, and lines 30-42 of Col. 7). Also note that Figure4 shows the amplitude of the input Vin2 about 1V (see input waveform in Figure 4) which is smaller than the power voltage (5V, see Figure 3) used for the data latch circuit.

With respect to claims 2, 25, 38, 48 and 61-64, Figure 3 of Tam discloses a data latch circuit for sampling a digital signal (Vin2, see Figure 4 in which input waveform is a digital

input signal), which includes: a capacitor means (C2) having first and second electrodes (right electrode and left electrode of C2); an inverter (Q1, Q11); a first switch (Q6); a second switch (Q10); and a third switch (Q8); wherein the first switch (SW3) and the second switch (Q10) are turned to input a first potential to the second electrode of the capacitor means (Q6 and Q8 are on to connected the second electrode of C2 to ground) during a reset period; and the digital signal (Vin2) is input to the second electrode of the capacitor means (C2) during a sampling period (Q6 and Q8 are off, and Q2 is ON) after the reset period. Note that the circuit in Figure 3 of Tam uses thin-film transistors and are used in display device (see lines 47 to line 60 of Col. 5, and lines 30-42 of Col. 7). Also note that Figure 4 shows the amplitude of the input Vin2 about 1V (see input waveform in Figure 4) which is smaller than the power voltage (5V, see Figure 3) used for the data latch circuit.

Insofar as understood of claims 14 and 15, it is seen that the reset period is controlled by a first signal (RST1) which controlling the switches Q6 and Q8, and the sampling period is controlled by a second signal (GO1) which controlling the switch Q10. Note that the recitations "a first sampling pulse from a first circuit" and "a second sampling pulse from a second circuit" are not part of the structure of the data latch circuit, so the above recitations are just and intended used, and it is seen in the operation of the Tam circuitry that the signals RST1 and GO1 are capable of receiving signals (pulses) from any source including from a first circuit and a second circuit, so the reset period and the sampling period are determined by first and second sampling pulses (because the reset period and the sampling period are not existed at the same time period).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 75-84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama et al. (US 2002/0021295 A1) in view of Tam (USP 6,628146).

With respect to claim 75, Figure 17 of the Koyama et al. reference discloses a semiconductor device, which includes: a shift register (all of SR in Figure 17) having at least a first circuit and a second circuit (for example, first and second SR in Figure 17); at least first and second data latch circuits (circuits LAT1) which sample a digital signal (Digital Data). The Koyama et al. reference does not disclose each of the first and second data latch circuits comprising a capacitor, an inverter, and a switch. However, the Tam reference discloses in Figure 6 a data latch circuit that reduces power consumption (Col. 4, lines 14-16 and Col. 5, lines 30-31) for sampling a digital signal (Vin2, see Figure 4 in which input waveform is a digital input signal), which includes: a capacitor (C2) having first and second electrodes (right electrode and left electrode of C2); an inverter (T1, T2); a switch (SW3) wherein the switch (SW3) is turned on and a first potential is input to the second electrode of the capacitor (when SW3 is turned on, so SW5 is also on to connected the second electrode of C2 to ground) during a reset period; and the digital signal (Vin2) is input to the second electrode of the capacitor means (C2) during a sampling period (SW3 is off, and SW2 is ON) after the reset period. Therefore, it would have been obvious to one having skill in the art at the time the invention was made to

modify the device in Figure 17 of the Koyama et al. reference by using the specific latch circuit as taught in Figure 2 of the Tam reference for each of the broad latch circuits LAT1 in Figure 17 of Koyama et al. for the purpose of reducing the power consumption of the device. Thus, this modification meets all the limitations of claim 75.

Insofar as understood in claim 76, the combination/modification as discussed in claim 75 having the structure of the shift register and the latches similar as application invention, so it meets the limitation that the reset period is determined from a first sampling pulse form the first circuit (first SR) and the sampling period is determined from a second sampling pulse from the second circuit (second SR).

With respect to claims 77-79, note that Figure 4 of Tam shows the amplitude of the input Vin2 about 1V (see input waveform in Figure 4) which is smaller than the power voltage (5V, note Figure 3 shows the supply voltage for Tam is 5V) used for the data latch circuit, and the circuit in Tam uses thin-film transistors. Note that the device in Figure 17 of Koyama et al. is used in display device (see abstract of Koyama et al.).

With respect to claims 80-84, the above combination/modification of Koyama et al. and Tam also meets all the limitations of this claim for the similar reasons as discussed in claims 75-79. Note that, the first switch (SW3), the second switch (SW5) and the third switch (SW2) are shown in Figure 6 of Tam.

8. Claims 75-84 are also rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama et al. (US 2002/0021295 A1) in view of Nakamura (US 2002/0075211 A1).

With respect to claim 75, Figure 17 of the Koyama et al. reference discloses a semiconductor device, which includes: a shift register (all of SR in Figure 17) having at least a

first circuit and a second circuit (for example, first and second SR in Figure 17); at least first and second data latch circuits (circuits LAT1) which sample a digital signal (Digital Data). The Koyama et al. reference does not disclose each of the first and second data latch circuits comprising a capacitor, an inverter, and a switch. However, the Nakamura reference discloses in Figure 13 a data latch circuit for sampling a digital signal (IN), which includes: a capacitor (C2) having first and second electrodes (right electrode and left electrode of C2); an inverter (53); a switch (SW3) wherein the switch (SW3) is turned on and a first potential is input to the second electrode of the capacitor (when SW3 is turned on, so SW1 is also on to connected the second electrode of C2 to 1.65V) during a reset period; and the digital signal (IN) is input to the second electrode of the capacitor means (C2) during a sampling period (SW3 is off, and SW2 is ON) after the reset period. Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the device in Figure 17 of the Koyama et al. reference by using the specific latch circuit as taught in Figure 13 of the Nakamura reference for each of the broad latch circuits LAT1 in Figure 17 of Koyama et al. for the purpose of converting a lower amplitude signal into a desired higher amplitude signal (paragraphs [0096]-[0097]. Thus, this modification meets all the limitations of claim 75.

Insofar as understood in claim 76, the combination/modification as discussed in claim 75 having the structure of the shift register and the latches similar as application invention, so it meets the limitation that the reset period is determined from a first sampling pulse form the first circuit (first SR) and the sampling period is determined from a second sampling pulse from the second circuit (second SR).

With respect to claims 77-79, note that because the data latch circuit in Figure 13 of Nakamura is converted a signal into higher amplitude (paragraph [0096]-[0097]) so it is inherent that the amplitude of the input signal IN is smaller than amplitude of the power voltage used for the data latch circuit, and the data latch circuit in Nakamura uses thin-film transistors. Note that the semiconductor device in Koyama et al. is used in display device (see abstract of Koyama et al.).

With respect to claims 80-84, the above combination/modification of Koyama et al. and Nakamura also meets all the limitations of this claim for the similar reasons as discussed in claims 75-79. Note that, the first switch (SW3), the second switch (SW1) and the third switch (SW2) are shown in Figure 13 of Nakamura.

Allowable Subject Matter

9. Claims 7, 8, 11, 12, 43, 44, 53, 54, 65, 66, 68-71, 73 and 74 are presently allowed.

Note that claims 20, 21, 30, 31, 67 and 72 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action because they depend on allowable claims 7, 8, 65 and 70.

10. Claims 85-96 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Response to Arguments

11. Applicant's arguments filed on 6/29/05 have been fully considered but they are not persuasive.

Note that applicant argues that Tam does not disclose or suggest a data latch circuit which samples a digital signal. However, this argument is not persuasive because the circuit in

Tam (see Figure 3, or 6) shows a data latch circuit (due the switch connected between the output of the inverter to the input of the inverter as discussed in the 102 rejection), and the input signal VIN2 is a digital input signal (see Figure 4 for the input waveform which is a digital signal). Further, "for sampling a digital signal" is merely an intended use and the circuit in Tam meets all the structure of the claim and thus it is capable of performing such intended use function.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

September 15, 2005

LONG NGUYEN
PRIMARY EXAMINER